WHAT IS CLAIMED IS:

1. A method for forming a magnetic memory cell junction, comprising:

patterning a mask layer above a stack of layers;

etching exposed portions of the stack of layers to a level spaced above a tunneling barrier layer of the stack of layers; and

implanting dopants into remaining portions of the stack of layers arranged above the tunneling barrier layer.

2. The method of claim 1, wherein the step of etching comprises etching one or more magnetic layers of the stack of layers.

3. The method of claim 2, wherein the step of etching comprises etching to a level within one of the magnetic layers.

4. The method of claim 1, wherein the step of etching comprises etching between approximately 20% and approximately 95% of a thickness of the stack of layers arranged above the tunneling barrier layer.

5. The method of claim 1, wherein the step of implanting comprises oxidizing the remaining portions of the stack of layers arranged above the tunneling barrier layer.

6. The method of claim 1, wherein the step of implanting comprises nitriding the remaining portions of the stack of layers arranged above the tunneling barrier layer.

7. The method of claim 1, wherein the step of implanting is adapted to prevent the introduction of dopants into portions of the stack of layers underlying the tunneling barrier layer.

8. The method of claim 1, wherein a magnetic layer underlying the tunneling barrier layer comprises a material adapted to prevent the introduction of dopants within the magnetic layer during the step of implanting.

9. A method for forming a magnetic memory cell junction, comprising:

patterning a mask layer above a stack of layers; and

alternately etching and implanting dopants into exposed portions of the stack of layers.

10. The method of claim 9, wherein the step of alternately etching and implanting comprises:

generating veils along sidewalls of the patterned stack of layers; and

implanting dopants into the veils.

11. The method of claim 10, wherein the step of alternately etching and implanting further comprises removing the doped veils.

12. The method of claim 9, wherein the step of alternately etching and implanting comprises etching a greater amount of the stack of layers than the amount of the stack of layers implanted with dopants during the step of implanting.

13. The method of claim 9, wherein the step of alternately etching and implanting comprises oxidizing the exposed portions of the stack of layers.

14. The method of claim 12, wherein the step of alternately etching and implanting further comprises nitriding the exposed portions of the stack of layers.

15. A magnetic memory cell junction comprising a tunneling barrier layer interposed between an overlying magnetic layer and an underlying magnetic layer, wherein the underlying magnetic layer comprises a material adapted to retard the implantation of dopants relative to a rate of dopant implantation within a material of the overlying magnetic layer.

16. The magnetic memory cell junction of claim 15, wherein the material of the underlying layer comprises cobalt-platinum.

17. The magnetic memory cell junction of claim 15, wherein the material of the underlying layer comprises cobalt-iron-boron.

18. The magnetic memory cell junction of claim 15, further comprising another underlying magnetic layer spaced below the tunneling barrier layer, wherein the other underlying magnetic layer comprises a material adapted to retard the implantation of dopants relative to a rate of dopant implantation within the material of the overlying magnetic layer.

19. The magnetic memory cell junction of claim 15, wherein a length of the overlying magnetic layer is shorter than a length of the underlying magnetic layer.

20. The magnetic memory cell junction of claim 15, wherein the underlying and overlying magnetic layers comprises substantially similar lengths.